1. A method of fabrication of etching a low -k dielectric layer used in microelectronics fabrication; comprising the steps of :

a) forming an organic low k dielectric layer over a substrate;

b) forming a masking pattern over said organic low k dielectric layer; said masking pattern having an opening;

c) using an etch process said organic low k dielectric layer through said opening using said resist pattern as an etch mask; said etch process comprising:

(1) in a first step, etching said organic low k dielectric layer by applying a plasma power and flowing at least NH_3 gas.

2. The method of claim 1 wherein said first step comprises applying a medium plasma power plasma density between 1E9 and 1E11 cm^{-3} and flowing only NH_3 gas.

3. The method of claim 1 wherein said first step comprises applying a medium plasma power plasma density between 1E9 and 1E11 cm^{-3} and flowing only NH_3 gas, a power in between 500 and 1500 W, and a NH_3 flow between 50 and 300 sccm and a pressure between 80 and 800 mTorr.

4. The method of claim 1 wherein said first step comprises applying a medium plasma power plasma density between 1E9 and 1E11 cm^{-3} and flowing only NH_3 gas, a power in between 500 and 1500 W, and a NH_3 flow between 50 and 300 sccm and a pressure between 80 and 800 mTorr and flowing CO or O_2 gasses.

5. The method of claim 1 wherein said organic low k dielectric is comprised of a material selected from the group consisting of fluorinated arylether, Benzocyclobuthene (BCB), amorphous teflon, carbon doped oxides, poly arylene ether (PAE) and organic Spin on materials.

6. The method of claim 1 wherein said organic low k dielectric is comprised of a material selected from the group consisting of fluorinated arylether, and poly arylene ether.

7. The method of claim 1 wherein said organic low k dielectric is comprised of carbon doped oxide.

8. The method of claim 1 wherein said organic low k dielectric is comprised of poly arylene ether (PAE).

9. The method of claim 1 wherein said etch forms a first opening through said organic low k dielectric layer; said first opening having sidewalls defined by said organic low k dielectric layer; said sidewalls are substantially vertical at a angle between 87 and 93 degrees to the surface of the substrate.

10. The method of Claim 1 wherein the substrate is selected from the group consisting of: microelectronics conductor materials; microelectronics semiconductor materials; and microelectronics dielectric materials.

11. A method of fabrication of etching a low -k dielectric layer, comprising the steps of :

a) forming an organic low k dielectric layer over an insulation layer over a substrate;

b) forming a masking pattern over said organic low k dielectric layer; said masking pattern having an opening;

c) using an etch process said organic low k dielectric layer through said opening using said masking pattern as an etch mask; said etch process comprising:

(1) in a first step, etching said organic low k dielectric layer by applying a plasma power and flowing NH_3 and H_2 etch gasses.

12. The method of claim 11 wherein said first step comprises: a plasma power between 500 and 1500 W, medium plasma power plasma density between 1E9 and 1E11 cm^{-3}, a NH_3 flow between 50 and 300 sccm, a H_2 flow between 50 and 300 sccm and a pressure between 80 and 800 mTorr.

13. The method of claim 11 wherein said first step comprises: a plasma power between 500 and 1500 W, medium plasma power plasma density between 1E9 and 1E11 cm^{-3}, a NH_3 flow between 50 and 300 sccm, a H_2 flow between 50 and 300 sccm and a pressure between 80 and 800 mTorr and flowing O_2 or CO gasses.

14. The method of claim 1 wherein said organic low k dielectric is comprised of a material selected from the group consisting of fluorinated arylether, Benzocyclobuthene (BCB), amorphous teflon, carbon doped oxides, poly arylene ether (PAE) and organic Spin on materials.

15. The method of claim 11 wherein said organic low k dielectric is comprised of a material selected from the group consisting of fluorinated arylether, and poly arylene ether.

16. The method of claim 11 wherein said organic low k dielectric is comprised of carbon doped oxide.

17. The method of claim 11 wherein said organic low k dielectric is comprised of poly arylene ether (PAE).

18. The method of claim 11 wherein said etch forms a first opening through said organic low k dielectric layer; said first opening having sidewalls defined by said organic low k dielectric layer; said sidewalls are substantially vertical at a angle between 87 and 93 degrees to the surface of the substrate.

19. A method of fabrication of etching a low -k dielectric layer; comprising the steps of:

a) forming an organic low k dielectric layer over a insulation layer over a substrate;

b) forming a masking pattern over said organic low k dielectric layer; said masking pattern having an opening;

c) using an etch process said organic low k dielectric layer through said opening using said masking pattern as an etch mask; said etch process comprising:

(1) in a first step, etching said organic low k dielectric layer by applying a plasma power and flowing only NH_3 and N_2 etch gasses.

20. The method of claim 19 wherein said first step comprises: power in between 500 and 1500 W, medium plasma power plasma density between 1E9 and 1E11 cm^{-3}, a NH_3 flow between 50 and 300 sccm and a N_2 flow between 50 and 300 sccm and a pressure between 80 and 800 mTorr.

21. The method of claim 19 wherein said first step comprises: power in between 500 and 1500 W, medium plasma power plasma density between 1E9 and 1E11 cm^{-3}, a NH_3 flow between 50 and 300 sccm and a N_2 flow between 50 and 300 sccm and a pressure between 80 and 800 mTorr and flowing CO or O_2 gasses.

22. The method of claim 19 wherein said organic low k dielectric is comprised of a material selected from the group consisting of fluorinated arylether, Benzocyclobuthene (BCB), amorphous teflon, carbon doped oxides, poly arylene ether (PAE) and organic Spin on materials.

23. The method of claim 19 wherein said organic low k dielectric is comprised of a material selected from the group consisting of fluorinated arylether, and poly arylene ether.

24. The method of claim 19 wherein said organic low k dielectric is comprised of carbon doped oxide.

25. The method of claim 19 wherein said organic low k dielectric is comprised of poly arylene ether (PAE).

26. The method of claim 19 wherein said etch forms an first opening through said organic low k dielectric layer; said first opening having sidewalls defined by said organic low k dielectric layer; said sidewalls are substantially vertical at a angle between 87 and 93 degrees to the surface of the substrate.